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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,690	KOCH, KENNETH E.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-146* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57, 66-102,108-126 and 137-146* is/are rejected.

7)☒ Claim(s) *58-65,103-107 and 127-136* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-146 are presented for examination.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/075,917. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons. Furthermore, claim 1 is generic to the species of invention covered by claim 1 of the patent. Thus, the generic invention is "anticipated" by the species of the patented invention. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim) . This court's predecessor has held that, without a terminal disclaimer, the species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller , 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claims 1,23 are properly rejected under the doctrine of

obviousness-type double patenting (see In re Goodman (CA FC) 29 USPQ2d 2010).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1, 66 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons given below.

4. As to claim 1, no physical transformation can be found in the claim. No substantial practical application can be fond in the clam . The practical application of the evaluation of the Normal Form Boolean expression/operations is not found. The plurality of input/output interfaces are operable to receiving the compile\d Boolean expressions/operations, and transmit the results. But, no practical application can be found for the compiled results. Therefore, the claim subject matter is not useful. The receiving and transmitting the expressions / operations and results is not tangible. Although claim further recites a plurality of registers, the practical application of the plurality of registers is not found.

5. As to claim 66, similarly, no substantial practical application can be fond for the starting , evaluating ,and selectively short circuiting the Boolean expression steps.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-16, 32-49, 53-56, 57-94, 96-100, 102-139 are rejected under 35 U.S.C. 102(b) as being anticipated by Saldanha et al. (5,682,519).

7. As to claims 1,2, 8, 32, Saldanha taught a processor comprising at least :

a) a Boolean logic circuit (see fig.5) , wherein the Boolean logic unit is operable for performing the short circuit evaluation of Normal Form Boolean expressions/operations (see AND gate, see the short circuited AND and OR in col.7, lines 53-65, see for Boolean expression);

b) a plurality of input/output interfaces (see fig.5) , wherein the plurality of input/output interfaces are operable for receiving plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results, and a plurality of registers (see Boolean expressions and compiled result in col.4, lines 48-67, col.5, lines 1-57, see also figs.4 , 7,8 for the input/output connections, see also the simulation of logic properties of the circuit and the Boolean expressions in col.2, lines 36-67 for background).

8. As to claims 3, 33, Saldanha also rolled up the results of the AND and OR gates (see figs.4,5).

9. As to claims 4,5, Saldanha also had default and initialized value of 1 (see "1" in fig.4).

10. As to claims 6,9, Saldanha also remained one on 0 result (see OR zero if the disjuncts were 0 value and the AND remained 1 in col.2, line 63, see also figs.5,7).

11. As to claim 7, see short circuited OR "1" in figs.5,7).

12. As to claim 10, Saldanha also included AND disjunct register to indicate the AND clause (see figs.5,7, see also the enable signal in fig.5).

13. As to claim 11, Saldanha also included AND disjunct register to initialize to 0 until the AND was "one" (see the enable AND 1 in figs.5,7,).

14. As to claim 12, Saldanha also included AND remain 1 until reset (see enable reset for the AND in col.8, lines 40-47)

15. As to claim 13, Saldanha also included conjunct evaluation to false if the AND register is set to "0" and the AND disjunct register is set to "0", and the processor short-circuits to the start of the next conjunct (see the short circuited AND in col.7, lines 40-65, see the iterations for the next conjunct).

16. As to claim 14,15, 57, Saldanha also included a at least one bit (see the X=0 for one bit for the AND , OR, see also Xi for multiple bits in col.5, lines 29-33).

17. AS to claim 16, Saldanha did not specifically show the decoder for deciphering the operational code as claimed. However, examiner holds that a decoder for decoding an operational code must have included in Saldanha because Saldanha also taught

a computer 142 including the memory and system processor (see col.5, lines 40-52). Therefore, a decoder for deciphering or decoding the operational code should be a standard component in the computer.

18. As to claim 34, Saldanha also included AND/OR register 1 when evaluating the conjunctive and 0 when evaluating disjunctive (see AND of logic 1 and OR 0 in fig.5 and fig.7).

19. As to claim 35 , Saldanha initializes to a value of one after the start of a predetermined operational code when evaluating Conjunctive Normal Form Boolean expressions/operations and a value of zero when evaluating Disjunctive Normal Form Boolean expressions/operations (see the true value of AND and false value of OR).

20. As to claim 36, Saldanha AND/OR register remains at a value 1 if all of the conjuncts of a Conjunctive Normal Form Boolean expression/operation being evaluated were true, and remains at a value of 0 if all of the disjuncts of a Disjunctive Normal Form Boolean expression/operation being evaluated were 0 (see AND and OR of input value 1 and 0 in fig.5).

21. As to claim 37, Saldanha taught conjunctive Normal Form Boolean expression/operation is false if the AND/OR register was 0 and the remainder of the Boolean expression/operation is short-circuited (see the short circuited AND OR in fig.5,7).

22. As to claim 38, Saldan taught a Disjunctive Normal Form Boolean

expression/operation was true if the p-bit AND/OR register was true and the remainder of the Boolean expression/operation is short-circuited (see the short circuited disjunctive Boolean AND and OR in fig.5,7).

23. As to claim 39, Saldanha also taught a q-bit AND/OR register operable for storing the results of the evaluation of one or more terms within conjuncts and disjuncts (see the AND and OR conjuncts and disjuncts in fig.5, fig,.7).

24. As to claim 40, Saldanha also taught OR conjunct/AND disjunct register, the OR conjunct/AND disjunct register indicated OR clause, an AND clause, has begun (see the starting function of the OR conjunct and AND disjunct in col.6, lines 45-67, see also fig.4).

25. AS to claim 41, Saldanha also initialized the OR conjunct/AND disjunct register 0 when evaluating Conjunctive Normal Form Boolean expressions/operations and remained in that state until an OR was 1 and to a value of 1 when Disjunctive Normal Form Boolean remains in that state until an AND to 0 (see initialized OR and AND until the OR input of 1 and AND input of 0 in fig.

26. As to claim 42, Saldanha also included a predetermined conjunct evaluated to true if the AND/OR register was 1 and the OR conjunct/AND disjunct register was 1,

and the processor short-circuits to the start of the next conjunct (see the short circuited to the next conjunct in col.7, lines 42-65, see fig.5).

27. As to claim 43, Saldanha also included a predetermined disjunct evaluated to false if the AND/OR register was 0 and the OR conjunct/AND disjunct was set and the processor short-circuits to the start of the next disjunct(see the short circuited to the next disjunct in col.7, lines 42-65, see fig.5) .

28. As to claims 44,45, Saldanha taught 1 bit wide and multiple bits (see xi).

29. As to claim 46, Saldanha also taught encoding the bits bus either in series or in parallel(see each Boolean gates in series and parallel nodes in fog.5, for encoding , see the reencoding circuit in the background teaching in col.2, lines 1-35).

30. As to claim 47, Saldanha did not explicitly show the control buffer operable for storing state change commands until the control encoder is clear . However, Saldanha already taught encoding for changing the state in the background art (see the reencdoing state of the circuit in col.2, lines 1-35). Therefore, Examiner holds that Saldanha must have a storage or the like to hold encoding state changing commands in order to perform his iterative functions.

31. As to claim 48, Saldanha taught a secondary device state random-access memory (see the disk drive for external device).

32. As to claim 49, Saldanha also taught one or more memory devices, wherein the one or more memory devices are operable for storing the states of a plurality of devices that the processor monitors and controls (See RAM and disk drive in fig.2).

33. As to claim 53, Saldanha also included random-access memory devices (see fig.2 RAM).

34. As to claim 54, Saldanha must have a compiled micro-program because it was directed a computer and memory with iterated program (see the iterated program flow in fig.2, 3a,b).

35. As to claim 55, no fetch of instruction has been taught by Saldanha. However, since Saldanha taught RAM and the program flow (see fig.2 and fig.3), it must have included fetching of instructions .otherwise , the program flow could not be executed.

As to claim 66, Saldanha. Also taught :

a) starting an operation related to a Normal Form Boolean expression, wherein the Boolean expression comprises a conjunct or a disjunct (see the root node and the conjuncts and the disjuncts of the AND and OR in fig.5);

b) evaluating the conjunct or disjunct (see col.5, lines 1-67, col.8, lines 10-1-63, see also example in fig.7); and

c) selectively short-circuiting a portion of the Boolean expression (see the short circuit in col.7, .lines 41-67, col.8, lines 1-13).

36. As to claim 67, Saldanha also included AND disjunct register to indicate the AND clause (see figs.5,7, see also the enable signal in fig.5).

37. As to claim 68, See OR operation in fig.5.

38. As to claim 69, 70,71, see disjuncts in AND in fig.5 (See also AND in col.2, lines 60-67).

39. AS to claim 72, see the logical 1 in col.2, lines 60-67.

AS to claim 73, , Saldanha also included a disjunct comprising an AND clause, ANDing the result of each AND operation with the current value of an AND register (see fig.5 X4 at the AND gate).

AS to claim 74, Saldanha also taught AND register had a value of 0 and an AND disjunct register is set to 1 , evaluating the disjunct to false and short-circuiting to a next disjunct (see short circuited AND 370 in fig.5).

AS to claim 75, Saldanha also taught an OR operation and the next disjunct and rolling the value of the AND register up to an OR register by OR'ing the value of the AND register the value of the OR register (see the short circuited OR in fig.5).
AS to claims 76,77, Saldanha also taught the AND-bit has a value of true when the OR operation is processed, changing the final OR- bit to a value of true (see OR output of 1 in fig.5) .
AS to claim 78, Saldanha also evaluated the conjunctive Boolean expression and disjunctive Boolean expression (see AND and OR in fig.4, for Boolean expression see col.2, lines 60-67, col.3, lines 1-13).
AS t claim 79, Saldanha also included separate conjuncts and disjuncts and separate Boolean processor (see the 240 conjunct normal form and 270 for the disjunct normal form fig.5).

40. As to claim 80, Saldanha also included a conjunct (see AND conjunct) in a first separate Boolean processor results in a false evaluation , providing a signal from the first separate Boolean processor to the other separate Boolean processors (see 270) , that the entire expression is false (see short circuited output).
41. As to claim 81, Saldanha also included a disjunct (see the OR) in a first separate Boolean processor results in a true evaluation, providing a signal, from the first separate Boolean processor to the other separate Boolean processors (260) , that the entire expression is true (see true evaluation of the OR disjunct in fig.5).
As to claim 82, Saldanha also taught at least :

a) a general-purpose processor (see computer in fig.1) ; and

b) a Boolean co-processor (see fig.5) that accepts code, representative of Boolean code, from the general-purpose processor, the Boolean processor including:

c) a Boolean logic unit, wherein the Boolean logic unit is operable for performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations, operable for performing the short-circuit evaluation of Disjunctive Normal Form Boolean expressions/operations, or operable for performing the short-circuit evaluation of both Conjunctive Normal Form Boolean expressions/operations and Disjunctive Normal Form Boolean expressions/ operations (see short circuited AND and OR in fig.5);

c) a plurality of input/output interfaces, wherein the plurality of input/output interfaces are operable for receiving a plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results (input/output interfaces not explicitly shown, but is shoed the compiled results 0 and 1 at the outputs) ; and

d) a plurality of registers.

42. As to claim 83, Saldanha also rolled up the results of the AND and OR gates (see figs.4,5).

43. As to claims 84,85, Saldanha also included default or initial value of the p-bit first register is one when evaluating Conjunctive Normal Form Boolean expressions/operations and 0 when evaluating Disjunctive Normal Form Boolean expressions/operations (see X4 to the short circuited conjunctive AND and OR).

44. As to claim 86, Saldanha also included a value of 1 if all of the conjuncts of a Conjunctive Normal Form Boolean expression/operation being evaluated pre true (see the conjuncts of AND), and wherein the p-bit register remains at a value of 0 if all of the disjuncts (see disjuncts of OR) of a Disjunctive Normal Form Boolean being evaluated are false (see output of OR 260 as 1 and output of OR 270 as 0).

45. As to claim 87, Saldanha also taught a Conjunctive Normal Form Boolean expression/operation was if the p-bit first register is set to 0 , and the remainder of the Boolean expression/operation is short-circuited false (see the short circuited AND in fig.5) .

46. As to claim 88, Saldanha also taught a Disjunctive Normal Form Boolean expression/operation was true if the p-bit first register is set to 1 and the remainder of the Boolean expression/operation is short-circuited (see short circuited OR) .

As to claim 89, Saldanha also taught a second register operable for storing the results of the evaluation of one or more terms within conjuncts and/or disjuncts (see Xi).

47. As to claim 90, Saldanha also taught a third register indicates that the evaluation of a conjunct comprising an OR clause, or a disjunct comprising an AND clause, has begun (see Xi inputs at AND and OR).

48. As to claim 91, Saldanha also initialized to a value of 0 when evaluating Conjunctive Normal Form Boolean expressions/operations (AND) and remains in that state until an OR value was 1 (see inputs to AND) , and initializes to a value of 1

when evaluating Disjunctive Normal Form Boolean expressions/operations (see OR) and remains in that state until an AND expression/operation sets its value to 1.

49. As to claim 92, Saldanha also included a predetermined conjunct evaluates to true if a second register was one (see x4) and third register was set to 1 (see output at short circuited AND) and the computing device short-circuited to the start of the next conjunct.

50. As to claim 93, a predetermined disjunct evaluates to false if the q-bit second register is set to 0 and a third register is set 1 , and the computing device short-circuits to the start of the next disjunct.

51. As to claim 94, Saldanha did not specifically show the decoder for deciphering the operational code as claimed. However, examiner holds that a decoder for decoding an operational code must have included in Saldanha because Saldanha also taught a computer 142 including the memory and system processor (see col.5, lines 40-52). Therefore, a decoder for deciphering or decoding the operational code should be a standard component in the computer.

AS to claim 96, see encoder in col.2, lines 1-30, for parallel bits , see parallel inputs x in fig.8).

52. AS to claims 97,98, see RAM and disk drive in fig.2.

53. As to claim 99, Saldanha must have a compiled micro-program because it was directed a computer and memory with iterated program (see the iterated program flow in fig.2, 3a,b).

54. As to claim 100, no fetch of instruction has been taught by Saldanha. However, since Saldanha taught RAM and the program flow (see fig.2 and fig.3), it must have included fetching of instructions .otherwise , the program flow could not be executed.

55. As to clam 102, see Xi registers.

AS to claim 108, Saldanha taught a hybrid processor, comprising:

a) a host processor, wherein the host processor is at least operable for performing comparison operations and register modifications (see computer in fig.2) ; and

b) a Boolean short-circuit outcome calculation unit (see fig.5) , wherein the Boolean short- circuit outcome calculation unit was operable for evaluating the short-circuit outcome of Conjunctive Normal Form Boolean expressions/operations (see the short circuit AND in fig.5)operable for evaluating the short-circuit outcome of Disjunctive Normal Form Boolean expressions/ operations (see the short circuit OR), or operable for evaluating the short-circuit outcome of both Conjunctive Normal Form Boolean expressions/operations and Disjunctive Normal Form Boolean expressions/operations;

c) a plurality of input/output interfaces operable for receiving from the host processor, data related compiled Boolean expressions/operations and transmitting (receiving and transmission not explicitly shown but it showed input bus and output bus in fig.5, see also system bus in fig.2 connected to the host computer) to the host processor, data representative of the short-circuit outcome of a plurality of evaluated Normal Form

Boolean expressions/operations (see the 0 and 1 outputs in the short circuit); and

d) a plurality of registers (see xi registers).

56. As to claim 109, Saldanha also rolled up the results of the AND and OR gates (see figs.4,5).

57. As to claim 110, Saldanha also included AND/OR register 1 when evaluating the conjunctive and 0 when evaluating disjunctive (see AND of logic 1 and OR 0 in fig.5 and fig.7).

58. As to claim 111 , Saldanha initializes to a value of one after the start of a predetermined operational code when evaluating Conjunctive Normal Form Boolean expressions/operations and a value of zero when evaluating Disjunctive Normal Form Boolean expressions/operations (see the true value of AND and false value of OR).

59. As to claim 112, Saldanha AND/OR register remains at a value 1 if all of the conjuncts of a Conjunctive Normal Form Boolean expression/operation being evaluated were true, and remains at a value of 0 if all of the disjuncts of a Disjunctive Normal Form Boolean expression/operation being evaluated were 0 (see AND and OR of input value 1 and 0 in fig.5).

60. As to claim 113, Saldanha taught conjunctive Normal Form Boolean expression/operation is false if the AND/OR register was 0 and the remainder of the Boolean expression/operation is short-circuited (see the short circuited AND OR in fig.5,7).

61. As to claim 114, Saldan taught a Disjunctive Normal Form Boolean

expression/operation was true if the p-bit AND/OR register was true and the remainder of the Boolean expression/operation is short-circuited (see the short circuited disjunctive Boolean AND and OR in fig.5,7).

AS to claims 115, 116, see enabling node in fig.5 and fig.7.

62. As to claim 117, Saldanha also taught OR conjunct/AND disjunct register, the OR conjunct/AND disjunct register indicated OR clause, an AND clause, has begun (see the starting function of the OR conjunct and disjunct in col.6, lines 45-67, see also fig.4).

63. AS to claim 118, Saldanha also initialized the OR conjunct/AND disjunct register 0 when evaluating Conjunctive Normal Form Boolean expressions/operations and remained in that state until an OR was 1 and to a value of 1 when Disjunctive Normal Form Boolean remains in that state until an AND to 0 (see initialized OR and AND until the OR input of 1 and AND input of 0 in fig.

64.

65. As to claim 119, Saldanha also included a predetermined conjunct evaluated to true if the AND/OR register was 1 and the OR conjunct/AND disjunct register was 1, and the processor short-circuits to the start of the next conjunct (see the short circuited to the next conjunct in col.7, lines 42-65, see fig.5).

66. As to claim 120, Saldanha also included a predetermined disjunct evaluated to false if the AND/OR register was 0 and the OR conjunct/AND disjunct was set and the processor short-circuits to the start of the next disjunct(see the short circuited to the next disjunct in col.7, lines 42-65, see fig.5) .

67. AS to claim 121, Saldanha did not specifically show the decoder for deciphering the operational code as claimed. However, examiner holds that a decoder for decoding an operational code must have included in Saldanha because Saldanha also taught a computer 142 including the memory and system processor (see col.5, lines 40-52). Therefore, a decoder for deciphering or decoding the operational code should be a standard component in the computer.

68. As to claim 122, Saldanha also taught one or more memory devices, wherein the one or more memory devices are operable for storing the states of a plurality of devices that the processor monitors and controls (See RAM and disk drive in fig.2).

69. As to claim 123, see RAM in fig.2.

70. As to claim 124, Saldanha must have a compiled micro-program because it was directed a computer and memory with iterated program (see the iterated program flow in fig.2, 3a,b).

71. As to claim 125, no fetch of instruction has been taught by Saldanha. However, since Saldanha taught RAM and the program flow (see fig.2 and fig.3), it must have included fetching of instructions .otherwise , the program flow could not be executed.

72. As to clam 126, see Xi register bits.

73. As to claim 137, see computer in fig.2.

74. As to claim 138, Saldanha also included a controlling register for controlling the conjunctive mode or disjunctive mode (see the enabling OR 330 and 360 in col.7, lines 42-65).

As to claim 139, Saldanha also included :

a) receiving a plurality of conditional tests (see the logic evaluation on each nodes in fig.4);

b) based upon the received plurality of conditional tests, generating an operation, in computer-readable format, representative of a Boolean expression in Conjunctive Normal Form or Disjunctive Normal Form (see the expression representing logic function in col.4, lines 46-67, col.2, lines 60-63 for basic expression of Boolean logic function) ;

c) storing the operation in a Boolean processor operable to evaluate the Boolean expression by processing the operation and to selectively short-circuit a portion of the Boolean expression (see the selecting of short circuit in col.5, lines 40-65, for the storage see RAM and disk drive in fig.2).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

75. Claims 140-146 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saldanha (5,682,519) in view of Jacobson et al. (6,608,771).

76. As to claim 140-146, limitations of parent claims have been discussed above. Saldanha did not specifically show the portion of most likely to create short circuit , nor the determination of the likelihood to create the short circuit as claimed. However, Jacobson taught a system for determining the chance of short circuit (see col.12, lines 52-67, see also the tag bits for indicating the possible short circuit in col.8, lines 44-53). It would have been obvious to one of ordinary skill in the art to use Jacobson in Saldanha for including the likelihood of short circuit as claimed because the sue of Jacobson could provide Saldanha the capability to predict possible condition of short circuit, thereby, reducing the power of the number of the circuit nodes , and Saldanha also taught the need for reducing the number of circuit components and power consumption (see col.3, lines 14-21), which was motivation of the need for determining the likelihood of the short circuit portions in order to achieve the minimized power consumption.

77. Claims 17-31, 56, 95 , 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saldanha et al. (5,682,519) in view of Shankar (4,876,640) .

78. As to claims 17, 56, 95,101, Saldanha did not specifically show the decoder comprising the unconditional jump , conditional jump as claimed. However, Shankar

taught a decoder comprising an AND Array for conditional testing , branch address generation, and a number of miscellaneous functions (see col.5, lines 9-21, se also the PROM as microsequencer for decoding the operational codes in col.3, lines 32-65). It would have been obvious to one of ordinary skill in the art to use Shankar in Saldanha for including the decoder comprising the unconditional and conditional jump as clamed because the use of Shankar could provide Saldanha the ability to adapt to specific conditions of the system from the system user, such as programmable functions, therefore increasing the flexibility for adjusting additional system requirements , and it could be readily done by reconfiguring the decoder of Shankar into Saldanha with modified control parameters (e.g. the variables of the function call, or operation codes), so that specific operating code of Shankar could be recognized by Saldanha in order to achieve the enhanced capability , and for doing so ,provided motivation. AS to the start and no operation, Saldanha also taught an enabling signal to controls eh starting /disabling of the logic circuit (see enabling signal in col.8, lines 40-63).

79. As to the features of comparison between a memory value with the immediate value from instruction or form a threshold value claim 18-31, examiner holds that comparison at a logic gate such as AND , OR, had to be from either a memory location or from instructions component, such as an operand. For example, if the input value were not from a storage location, it must be from an operand designated by instruction. Since Saldanha already taught logic AND and OR comparisons by the program flow (see fig.3), the input values either be form a memory (see system memory shown in

fig,1 [146] p[147] or from the instruction into system. As to whether one value is grater or less than the other input, it is an inherent characteristic in a logic comparison. For example, a comparison logic gate had to determine the greater or lesser input value such as 0 or 1.

80. AS to claim 21, Saldanha did not specifically show the decoder for deciphering the operational code as claimed. However, examiner holds that a decoder for decoding an operational code must have included in Saldanha because Saldanha also taught a computer 142 including the memory and system processor (see col.5, lines 40-52). Therefore, a decoder for deciphering or decoding the operational code should be a standard component in the computer.

81. As to claim 18-20, 22 -28, see OR and AND gate evaluation in figs.4,5.

82. As to claims 29-31, see RAM in fig.2.

83. Claim 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saldanha (5,682,519) in view of Edwards et al. (5,271,019).

84. As to claim 50, Saldanha did not specifically teach his random-access memory included at least one bit associated with each memory location, and least one bit was operable for indicating the device state stored in the respective memory location was in the process of being modified. However, Edwards taught a bit for indicating the change state of a device (latch) toggled in a RAM (col.3, lines 15-26) . It would have

been obvious to one of ordinary skill in the art to use Edwards in Saldanha for including a bit in the RAM for indicating the respective memory location being modified as claimed because the use of Edwards could p[provide Saldanha the ability to update and recover the device state stored in a memory , and it could be achieved by defining the RAM memory of Edwards into the configuration file of Saldanha with modified control parameters (e.g. the bit type, bit status) so that specific bit for indicating device state of Edwards could be recognized by Saldanha, and because Saldanha also taught a RAM memory , although no specific details of RAM being disclosed, one of ordinary skill in the art should be able to recognize that the RAM could be used for storing the state of Saldanha's logic gates in order to achieve the iterative function of the short circuited path , and for doing so, provided a motivation.

85. As to claim 51, Edwards also included clearing the bit in the memory (see toggle bit).

86. As to claim 52, Edwards was also applicable for preventing the reading of the device state (se e the halt signal in col.7, lines 26-44).

87. Claims 58-65,103-107, 127-136 are objected to as being dependent upon a rejected base claim, but would be allowable, upon pending conditions of "101" if applicable, if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined detailed features of the instruction register, the first address register, the second address register and the short circuit functions of the Boolean logic unit .

88. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Gupta (6,385,757) is cited for the teaching of the address register and instruction registers (see col.44, lines 43-61, see also fig.14).

b) Mansfield , Jr. et al. (5,530,939) is cited for the background teaching of the short circuited evaluation of the Boolean AND and OR (see col.5, lines 26-44).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

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